CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES
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Memory cell 102D also includes storage capacitor 119 for storing data in the cell. A first plate 110' of capacitor 119 for memory cell 102D is integral with second source/drain region 110 of access transistor 111. Thus, memory cell 102D may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between second source/drain region 110 and capacitor 119. Surface 117 of second source/drain region 110 comprises a "micro-roughened" surface. This micro-roughened surface is formed by coating second source/drain region 110 with poly-silicon and treating the poly-silicon so as to form pores in surface 117. This increases the surface area of second source/drain region 110 and, thus, increases the capacitance of capacitor 119. The pores in surface 117 can be formed, for example, using the etching techniques described below.